This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An overlay target for optically measuring the overlay alignment of layers formed on a semiconductor comprising:

first and second test patterns, each including an upper grating layer and a lower grating layer, each grating layer including a series of substantially parallel lines, the upper grating lines of each test pattern aligned to be substantially parallel to the lower grating lines of the same test pattern, each test pattern having an associated offset bias defined by the lateral offset of the upper and lower grating layers of the test pattern, where a single line pitch is used for all gratings in all test patterns and where the difference between the offset bias of the first test pattern and the offset bias of the second test pattern is substantially equal to the line pitch divided by four whereby the combined optical response to the measurement of the first and second test patterns is sensitive to all values of overlay alignment.

2. (Original) An overlay target as recited in claim 1, wherein the magnitude of the offset bias of the first test pattern is equal to the line pitch divided by eight

3. (Original) An overlay target as recited in claim 1, wherein the upper and lower grating lines of the first test pattern are substantially parallel to the upper and lower grating lines of the second test pattern.

4. (Original) An overlay target as recited in claim 1, that further comprises:

a third test pattern, including an upper grating layer and a lower grating layer, each grating layer including a series of substantially parallel lines, the lines of the upper and lower gratings of the third test pattern aligned to be substantially parallel to each other, where the lines in the third test pattern are spaced at the same line pitch used for the first and second test patterns.

5. (Original) An overlay target as recited in claim 4, where the grating lines of the first, second and third test patterns have three different angular orientations in the plane of the wafer.

Claims 6-13. (Canceled)